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EXAMINER	
TRAN, NHAN T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/624,509	TAKAYANAGI, ISAO	
	Examiner	Art Unit	
	NHAN T. TRAN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-11,51-55,57-59 and 62-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *51* is/are allowed.

6)☒ Claim(s) *1-4, 6-11, 52-55, 57-59, 62-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-4, 6-11, 52-55, 57-59, 62-66 have been considered but are moot in view of the new ground of rejection.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 6 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The method claim 6 is not tied to a particular machine or apparatus. The claim simply requires steps without being processed by any particular machine or apparatus to produce a result or transform a particular article to a different state or thing. In the instant claim, the process steps can simply be memorized and performed by human but not a machine or apparatus. Although the preamble of claim 1 recites “an imager chip”, there is no interrelationship among the camera and the process steps in the body of the claim.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-4, 62 & 63 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 recites "wherein the background signal is not filtered before it is subtracted from the image signal." However, the specification does not provide support for this limitation. In fact, the background image is captured (read) from "no data" area of the memory disk 305, and then the **optical shading or fixed pattern noise** is stored in the memory array 403 as a **background signal component** (see paragraph [0028]). It is inherent that the background signal component is **not the same** as the background image but it is an extracted noise/shading component to represent noise/optical shading from the background image. Thus, in order to remove the noise from an image signal by the data subtraction 404 (Fig. 4), the background image must be somewhat filtered to extract the noise or optical shading component because there is no method to directly subtract an image (target image) from the background image without extracting the noise or optical shading component prior to the subtraction. Otherwise, the entire image pixel level from the target image would be improperly compensated by the subtraction. This is also clearly seen in Fig. 11 of the disclosure (where the memory unit 1008 is equivalent to a unit of the memory array 403 in Fig. 4) that background image is filtered by the time-domain low pass filter 1111 (see paragraph [0046]). Therefore, claimed subject matter of claim 1 is not supported by the specification.

Regarding claims 2-4, 62 & 63, these claims are also rejected as being dependent from claim 1.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 52-55, 64 & 65 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 52 recites "a pixel array circuit for outputting **an image signal including a background only signal**" and then "a data subtraction circuit, coupled to said memory array circuit and said pixel array circuit for performing a data subtraction **to remove said background only signal from said image signal using said stored background only signal**." This subtraction renders invalid image data or zero image data since the image of the background only is subtracted from itself. Therefore, the scope of the claim cannot be ascertained.

Claims 53-55, 64 and 65 are also rejected as being dependent from claim 52.

Note that the rejection of the following claims are based on best understood in view of the 35 USC 112 rejection above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 4, 52, 62-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dai et al. (US 6,763,142).

Regarding claim 1, Dai discloses an imaging device (Fig. 1), comprising:

a pixel array circuit (CCD array 20) that outputs an image signal including and a background signal caused by at least one of non-uniformity of illumination and optical shading, where the optical shading occurs during the collection of light (the target image inherently contains optical aberration noise known as non-uniformity of illumination or optical shading during capturing the image; see col. 1, lines 35-37 and col. 5, lines 14-31);

a memory array circuit (24 in Fig. 1), coupled to said pixel array circuit, to store the background signal;

a data subtraction circuit (27 in Fig. 1), coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction operation on the pixel array output to remove said background signal from said image signal (see col. 1, lines 6-10; col. 4, lines 11-17 and col. 5, lines 45-56).

Dai does not teach that the background signal is not filtered before it is subtracted from the image signal.

However, Dai suggests that various changes and alterations can be made to the embodiments (col. 5, lines 56-60).

Therefore, it would have been obvious to one of ordinary skill in the art to eliminating any filtering process of the background signal before it is subtracted from the image signal to simplify the circuitry and potentially increase processing speed.

Regarding claim 4, as disclosed by Dai, the memory array 24 stores the whole frame of background image (col. 5, lines 5-6, 21-23). Thus, each memory element in said memory array corresponds to a pixel circuit in said pixel array circuit.

Regarding claim 52, this claim is also met by the analysis of claim 1 above.

Regarding claims 62 & 65, Dai clearly discloses that the background signal further comprises a fixed pattern noise signal (col. 4, lines 11-17).

Regarding claims 63 & 64, Dai also discloses that the background signal, collected from the pixel array circuit, is captured from a no-data of a memory disk (col. 4, lines 32-40, wherein the short term memory 24 shown in Fig. 1 represents the memory disk, and the fixed pattern noise is stored in a no-data of the memory by inherency because signal can only be stored in a no-data area (empty area) of the memory).

9. Claims 2, 3, 6-11, 53, 54, 57-59 & 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dai et al. (US 6,763,142) in view of Goren (US 5,734,152).

Regarding claim 2, Dai does not explicitly disclose an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit. However, as taught by Goren, an edge enhancement filter (30 in Fig. 2a) is provided after a differentiator circuit (4) and before a digital circuit (20 in Fig. 1a) so that the edges of captured image signal are much more pronounced and it is much easier to digitize and decode such an enhanced signal (see col. 8, lines 15-18).

Therefore, it would have been obvious to one of ordinary skill in the art to implement an edge enhancement circuit after the subtraction circuit so that the edges of captured image signal are much more pronounced and it is much easier to digitize and decode such an enhanced signal as taught by Goren.

Regarding claim 3, Dai in view of Goren also discloses that the imaging device comprises an analog-to-digital converter (20 in Fig. 1a of Goren) which converts the signal received from the image enhancement circuit to a digital signal.

Regarding claim 6, the combined teaching of Dai and Goren as discussed in claim 1 also meets the method claim 6 *except* for "an imager chip" that is understood as an integrated imaging circuit for implementing the method. However, an Official Notice is taken that it is notoriously well known in the art to integrate an image sensor with image processing modules into a single chip for reducing size of circuitry for a compact apparatus.

Therefore, it would have been obvious to one of ordinary skill in the art to construct an imager chip that would implement the method for processing the image data as claimed to reduce circuit size, thereby providing a compact apparatus.

Regarding claim 7, Dai and Goren as discussed in claim 6 further discloses that the analog image data is received from a pixel array (CCD) in said imager chip.

Regarding claim 8, Dai and Goren as discussed in claim 6 also discloses that the analog image data is received from a memory array (24 in Dai) in said imager chip.

Regarding claim 9, it is seen from Iwai that the optical black signal in Iwai is considered as an offset variation signal since it is used as an offset to remove the dark shading (col. 7, lines 9-15).

Regarding claim 10, as disclosed by Dai, the background signal also includes a fixed pattern noise signal (see Dai, col. 5, lines 14-19).

Regarding claim 11, this claim is also met by the analysis of claim 3.

Regarding claims 53 & 54, these claims are also met by the analyses of claims 2 & 3, respectively.

Regarding claim 57, this claim is also met by the analyses of claims 1, 4 & 6 above, wherein "an integrated circuit" is the imager chip and "a substrate" is inherent (i.e. silicon substrate) in the imager chip.

Regarding claims 58, 59 & 66, these claims are also met by the analyses of claims 2, 3 & 10, respectively.

Allowable Subject Matter

10. Claim 51 is allowed.

The reason for allowance has been stated in the Applicant's remarks filed 1/4/2008.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NHAN T. TRAN whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NHAN T TRAN/
Primary Examiner, Art Unit 2622